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10/665,290	09/22/2003	Ingemar Soderquist	69993-254193	5630

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EXAMINER	
FENNEMA, ROBERT E	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/665,290	SODERQUIST ET AL.	
	Examiner	Art Unit	
	Robert E. Fennema	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 November 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-7 and 10 have been considered. Claim 1 amended as per Applicant's request.

Claim Objections

2. Claim 1 is objected to in light of the current amendment. The last section of text in the claim, after the amendments, reads "...an input signal or a completion of processing from a previous event the operation code comprises..." There appears to be a missing transition, as "the operation code comprises" does not appear to flow from the previous statement. Examiner has assumed an "; and" between these sections in terms of readability.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Knapp et al. (USPN 5,826,072, herein Knapp).

5. As per Claim 1, Knapp teaches: A digital signal processor comprising:

an instruction memory (Column 5, Lines 56-58), a central arithmetic unit (Column 6, Lines 10-12, the ALU), a register (Column 5, Lines 61-62), a controller (Column 5, Lines 62-63, the interrupt control logic), an event control unit (Column 5, Line 64 – Column 6, Line 5. For the remainder of this office action, it is assumed that the "event control unit" not only executes in a reaction to an event, but also is also the part of the processor that executes and/or schedules all instructions. This assumption is made by viewing Page 2, Lines 29-32 of the specification, where it appears that the event control unit is also responsible for executing or scheduling the "time performance constraints", in addition to the events) and input/output devices (Column 6, Line 1);

the instruction memory is arranged to include operation code including logical operations (Column 5, Lines 56-58), time performance constraints (Column 2, Lines 25-27) and events (Column 5, Line 64 – Column 6, Line 5);

the controller is arranged to suspend further processing of time performance constraints after initiating operations in an event control unit (Column 5, Line 64 – Column 6, Line 5. When the event (the interrupt in this case) is activated, it is run, and afterwards, the original instructions can resume running. By having to return to where the program was interrupted, it is clear that Knapp halts execution of the instruction flow during the interrupt) and resume processing when advised by the event control unit (Column 10, Lines 10-14, the return from interrupt instruction, where it has been stated above that the event control unit is interpreted to also include scheduling functions, such as scheduling a return from interrupt);

the event control unit is arranged to recognize an event that initiates or resumes processing, wherein the event is an input signal or a completion of processing from a previous event (Column 5, Lines 64-67, the signal is the interrupt request signal being activated) the operation code comprises an event operand arranged to identify the input signal or previous event to initiate or resume processing of the event control unit (Column 5, Lines 64-67) and a delay operand comprising those time performance constraints executed by a counter in the event control unit (Column 15, Lines 15-21, interrupts are stopped for 4 clock cycles after an interrupt occurs, and a counter is inherent to be able to keep track of those cycles, also see Column 23, Lines 14-15 and 21-23, other instructions halt interrupts also);

wherein the event control unit includes a package controller, a buffer register operable to store operands of a pulse package associated with a current operation code (Column 7, Line 35, the shadow registers) and an active register operable to store the operands of a pulse package associated with the previous operation code (Column 7, Lines 33-34, the main registers) wherein the package controller controls the transfer of operands to the buffer register (Column 7, Line 35) and from the buffer register to the active buffer (Column 15, Lines 11-16, on an interrupt, values are swapped between the main registers and the buffer registers, meaning data is going from one to the other and vice versa).

6. As per Claim 2, Knapp teaches: A digital signal processor in accordance with claim 1, wherein the event (Column 5, Lines 61-63. The interrupt control logic functions

as a detector, as it receives interrupt request signals, and as shown in Column 6, Lines 2-5, responds to the event as a consequence of those signals being detected) is detected by the event control unit (Column 5, Line 64 – Column 6, Line 9).

7. As per Claim 3, Knapp teaches: A digital signal processor in accordance with claim 2, wherein the event control unit is arranged to detect input signals (inherent that the control logic would be able to differentiate between a logic "0" and "1" on a signal line).

8. As per Claim 4, Knapp teaches: A digital signal processor in accordance with claim 2, wherein a further event is recognized as a completion of the processing carried out as a consequence of a previous event (Column 10, Lines 11-14, where there needs to be an explicit signal (or instruction) to end an interrupt).

9. As per Claim 5, Knapp teaches: A digital signal processor in accordance with claim 1, wherein the event is recognized as a completion of the processing carried out as a consequence of a previous event (Column 10, Lines 11-14, where there needs to be an explicit signal (or instruction) to end an interrupt).

10. As per Claim 6, Knapp teaches: A digital signal processor in accordance with claim 1, wherein the event control unit includes a signal memory arranged to store and

extract data under control of the event control unit (Column 6, Lines 26-29, data memory 90).

As per Claim 7, Knapp teaches: A digital signal processor in accordance with claim 6, wherein the signal memory is a vector memory (Column 12, Lines 65-66 show that the memory can be a "vector memory").

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Knapp, in view of Patterson et al. (herein Patterson).

13. As per Claim 10, Knapp teaches A digital signal processor in accordance with claim 1, but fails to teach: including two or more event control units arranged to work independently from each other.

However, Patterson teaches the idea of making a processor superscalar. A superscalar processor can execute multiple instructions at the same time, as long as they remain independent of each other (Pages 278-279). As assumed in the Claim 1

rejection, an "event control unit" appears to be a general execution unit, as it appears to work on all kinds of instructions in the processor. As shown in Patterson, and as one of ordinary skill in the art would recognize, the advantage of parallel processing is to increase performance by decreasing the cycles per instruction of the processor (Page 278). Given this advantage, it would have been obvious to one of ordinary skill in the art to apply the knowledge of superscalar processors to Knapps invention, and apply the same mechanic to the event control units, to allow for multiple units to execute simultaneously and independently for increased overall performance.

Response to Arguments

1. Applicant's arguments with respect to claim 1 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

2. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert E. Fennema whose telephone number is (571) 272-2748. The examiner can normally be reached on Monday-Friday, 8:45-6:15.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Robert E Fennema
Examiner
Art Unit 2183

RF

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